Antonio Becerra Esteban on

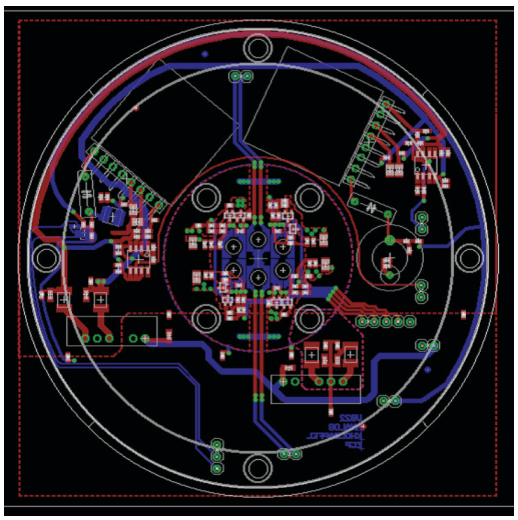
Common Pitfalls for Junior Designers

Early in my career, I was embarking on the intricate task of crafting the power management segment for a board designed to regulate rapid LED drivers and a photodiode for photon emission calibration.

I quickly found myself navigating the labyrinth of electronics engineering. At the heart of this sophisticated board lay an FPGA (Field Programmable Gate Array), the handiwork of a more seasoned colleague, leaving me to grapple with the complexities of power management...

Ploughing Through Datasheets

My quest began with a deep dive into the repositories of Mouser, Digikey, and RS Components, where I stumbled upon an application that seemed a beacon of promise. With optimism, I began the process of schematic capture. However, an issue quickly arose with the integrated circuit (IC).



Layout of the analog board with power management (for the analog signals), light emission, detection and signal amplification.

Early Learnings

My novice status meant I was oblivious to the fact that datasheets often represent a singular package variant of an IC, which may be available in multiple packages. Consequently, my schematic failed to accurately mirror the application for my chosen package, culminating in a board that was doomed from its inception. It sputtered to life once, only to be swiftly extinguished by a capacitor I had unwittingly sentenced to a fiery demise due to my schematic-induced short circuit.

While embarrassing, mistakes like these are common. They represent the dent of human errors made when interacting with such detailed documents like datasheets. These errors can spread and create more complex consequences when we transfer them to the schematic using an EDA tool.

Antonio studied physics at the University of Granada (Spain) and holds a Masters' degree in Applied Physics and Engineering of the Technical University of Munich (Germany). Before joining CELUS, he held roles in the semiconductor and EDA industries.

The Solution: CELUS

To shield engineers from these all-too-human pitfalls, my company has ushered in the CELUS Design Studio. This technological ally empowers engineers to transcend the traditional schematic capture process. By simply inputting their hardware architecture, the platform harnesses the power of automation to scour for the most compatible applications, weaving together an EDA project where each connection is meticulously curated.

This innovation not only safeguards against the errors of human oversight but ensures that no capacitor meets an untimely end due to an errant short circuit ever again. In my role as Manager of a team of application engineers, I am more than happy to provide you with further insights and advice regarding the CELUS Design Platform.

Now it's your turn! We are providing our technology for free to all our peer engineers out there to relieve you of the hassles and manual work you encounter day-to-day.

Sign Up Now

CELUS GmbH
Ridlerstraße 57, 80339 München
+49 (0)89 2555 2424 · info@celus.io
celus.io